

## WEST Search History





DATE: Saturday, November 12, 2005

<u>Hide?</u>	<u>Set Name Query</u>	<u>Hit Count</u>
	<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L28 (L15 or L23 or nop or noop or no-op) same reorder buffer\$1	2
	<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L27 (L19 or L26 or nop or noop or no-op) and reorder buffer\$1	0
<input type="checkbox"/>	L26 ("no operation" or "no-operation")	1655
	<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L25 (L19 or L23 or nop or noop or no-op) same reorder buffer\$1	2
<input type="checkbox"/>	L24 (L19 or L23 or nop or noop or no-op) with reorder buffer\$1	1
<input type="checkbox"/>	L23 ("no operation" or "no-operation")	11441
<input type="checkbox"/>	L22 nop with compress\$3	48
	<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L21 nop with compress\$3	8
<input type="checkbox"/>	L20 L19 adj (flag\$1 or indicator\$1)	0
<input type="checkbox"/>	L19 "non operation" or "non-operation"	3781
<input type="checkbox"/>	L18 ("no operation" or "no-operation") adj (flag\$1 or indicator\$1)	0
	<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L17 ("no operation" or "no-operation") adj (flag\$1 or indicator\$1)	6
<input type="checkbox"/>	L16 L15 adj (flag\$1 or indicator\$1)	6
<input type="checkbox"/>	L15 "non operation" or "non-operation"	3949
<input type="checkbox"/>	L14 buffer\$1 with L13	9
<input type="checkbox"/>	L13 nop with flag\$1	139
<input type="checkbox"/>	L12 nop with indicator\$1	15
	<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L11 nop with indicator\$1	2
<input type="checkbox"/>	L10 nop with flag\$1	11
<input type="checkbox"/>	L9 L7 or L8	3
<input type="checkbox"/>	L8 nop indicator\$1	1
<input type="checkbox"/>	L7 nop flag\$1	2
	<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L6 nop flag\$1	18
<input type="checkbox"/>	L5 nop indicator\$1	2
<input type="checkbox"/>	L4 fold\$3 with nop	9

<input type="checkbox"/>	L3	l1 with L2	148
<input type="checkbox"/>	L2	onchip or on-chip	28153
<input type="checkbox"/>	L1	dram with cache	4143

END OF SEARCH HISTORY

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**Key:** IEEE JNL = IEEE Journal or Magazine, IEEE JNL = IEEE Journal or Magazine, IEEE CNF = IEEE Conference, IEEE CNF = IEEE Conference, IEEE STD = IEEE Standard

1. **The cache DRAM architecture: a DRAM with an on-chip cache memory**  
Hidaka, H.; Matsuda, Y.; Asakura, M.; Fujishima, K.;  
Micro, IEEE  
Volume 10, Issue 2, April 1990 Page(s):14 - 25  
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2. **An experimental 1-Mbit cache DRAM with ECC**  
Asakura, M.; Matsuda, Y.; Hidaka, H.; Tanaka, Y.; Fujishima, K.;  
Solid-State Circuits, IEEE Journal of  
Volume 25, Issue 1, Feb. 1990 Page(s):5 - 10  
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3. **A circuit design of intelligent cache DRAM with automatic write-back capability**  
Arimoto, K.; Asakura, M.; Hidaka, H.; Matsuda, Y.; Fujishima, K.;  
Solid-State Circuits, IEEE Journal of  
Volume 26, Issue 4, April 1991 Page(s):560 - 565  
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4. **An experimental 1Mb cache DRAM with ECC**  
Asakura, M.; Matsuda, Y.; Hidaka, H.; Tanaka, Y.; Fujishima, K.; Yoshihara, T.;  
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IEEE CNF

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